2182

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the **PATENT APPLICATION** of:	
	Gredone et al.
Application No.:	10/081,466
Confirmation No.:	2915
Filed:	February 22, 2002
For: BASE STATION HAVING A HYBRID PARALLEL/SERIAL BUS INTERFACE	
Group:	2182
Examiner:	Abdelmoniem I. Elamin

Our File: I-2-0201.1US

Date: August 17, 2004

COMMUNICATION RE FAVORABLE IPER BY IPEA/US IN CORRESPONDING INTERNATIONAL APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This communication is to advise the Examiner of the favorable International Preliminary Examination Report (IPER) issued by the United States Patent and Trademark Office acting as International Preliminary Examination Authority in a corresponding international application. A copy of the IPER is enclosed.

The original PCT claims correspond to the claims in this U.S. application. A copy of the approved claims as published is also enclosed.

In view of the fact that PCT claims 1-37 have all been found to meet the international standards of patentability, prompt examination and allowance are respectfully requested.

Respectfully submitted,

Gredone et al.

By_____
Louis Weinstein
Registration No. 20,477
(215) 568-6400

Volpe and Koenig, P.C.
United Plaza, Suite 1600
30 South 17th Street
Philadelphia, PA 19103

LW/ns
Enclosures (2)

CLAIMS

What is claimed is:

1. A hybrid serial/parallel bus interface for a base station comprising:

a data block demultiplexing device having an input configured to receive a data block and demultiplexing the data block into a plurality of nibbles, each nibble having a plurality of bits;

for each nibble:

a parallel to serial converter for converting that nibble into serial data;

a line for transferring that nibble serial data; and

a serial to parallel converter for converting that nibble serial data to recover that nibble; and

a data block reconstruction device for combining the recovered nibbles into the data block.

2. The base station interface of claim 1 wherein a number of bits in a data block is N and a number of the lines is i and $1 < i < N$.

3. The base station interface of claim 1 wherein a number of bits in a nibble is four and a number of lines is two.

4. A hybrid serial/parallel bus interface for a base station comprising:

means having an input configured to receive a data block for demultiplexing the data block into a plurality of nibbles, each nibble having a plurality of bits;

for each nibble:

means for converting that nibble into serial data;

a line for transferring that nibble serial data; and

means for converting that nibble serial data to recover that nibble; and

means for combining the recovered nibbles into the data block.

5. The base station interface of claim 4 wherein a number of bits in a data block is N and a number of the lines is i and $1 < i < N$.

6. The base station interface of claim 4 wherein a number of bits in a nibble is four and a number of lines is two.

7. A base station having hybrid serial/parallel bus interface for transferring data from a first node to a second node, the interface comprising:

a data block demultiplexing device for demultiplexing a data block from the first node into m sets of n bits and for adding a start bit to each of the m sets, the m start bits collectively representing one of a particular function to be performed or a destination;

for each of the m sets, a separate line for transferring that set of the m sets from the first node to the second node;

a data block reconstruction device for receiving the m sets, for combining the m sets into the data block and for utilizing the m sets in accordance with the m start bits.

8. The base station interface of claim 7 wherein the demultiplexing device sets at least one of the m start bits in a one state when transmitting data and when the interface is not transmitting data, maintains all the separate lines in a zero state.

9. The base station interface of claim 7 wherein the m start bits represent a start of data transfer.

10. The base station interface of claim 7 wherein the m start bits collectively represent a particular function to be performed and not a destination.

11. The base station interface of claim 7 wherein functions that the m start bits collectively represent include a relative increase, a relative decrease and an absolute value function.

12. The base station interface of claim 7 wherein the m start bits collectively represent a particular destination and not a function to be performed.

13. The base station interface of claim 12 wherein destinations that the m start bits collectively represent include an RX and TX gain controller.

14. The base station interface of claim 7 wherein the m start bits collectively represent both a particular function to be performed and a particular destination.

15. A base station having a hybrid serial/parallel bus interface for transferring data from a first node to a second node, the interface comprising:

means for demultiplexing a data block into m sets of n bits;

means for adding a start bit to each of the m sets, the m start bits collectively representing one of a particular function to be performed or destination;

means for transferring from the first node each of the m sets over a separate line;

means for receiving at the second node each of the transferred m sets; and

means for utilizing the received m sets in accordance with the m start bits.

16. The base station interface of claim 15 wherein the adding means sets at least one of the m start bits to a one state and when the interface is not transmitting data, all the separate lines to a zero state.

17. The base station interface of claim 15 wherein at least one of the m start bits represents a start of data transfer.

18. The base station interface of claim 15 wherein the m start bits collectively represent a particular function to be performed and not a destination.

19. The base station interface of claim 15 wherein functions that the m start bits collectively represent include a relative increase, a relative decrease and an absolute value function.

20. The base station interface of claim 15 wherein the m start bits collectively represent a particular destination and not a function to be performed.

21. The base station interface of claim 20 wherein destinations that the m start bits collectively represent include an RX and TX gain controller.

22. The base station interface of claim 15 wherein the m start bits collectively represent both a particular function to be performed and a particular destination.

23. A base station hybrid serial/parallel bus interface for use in a synchronous system, the synchronous system having an associated clock, the bus interface, comprising:

a data block demultiplexing device having an input for receiving a data block and demultiplexing the data block into a plurality of nibbles, each nibble having a plurality of bits;

an even and an odd set of parallel to serial (P/S) converters, each set of P/S converters receiving the nibbles synchronous with a clock rate of the clock, and for converting the nibbles into a serial data;

a first set of i multiplexers for serially transferring data from the set of even P/S converters on a positive edge of the clock over i lines and serially transferring data from the set of the odd P/S converters on a negative edge of the clock over i lines;

a second set of i demultiplexers for receiving the even and odd serial data and sending the even received serial data to an even buffer and the odd serial data to an odd buffer;

an even and an odd set of serial to parallel (S/P) converters, the even set of S/P converters converting the received even serial data to even parallel data and outputting the even parallel data synchronous with the clock;

the odd set of S/P converters for converting the odd received serial data to odd parallel data and outputting the odd parallel data synchronous with the clock; and

a data block reconstruction device for combining the even and odd parallel data as the data block.

24. The base station interface of claim 23 wherein each data block has N bits and $1 < i < \frac{N}{2}$

25. The base station interface of claim 23 wherein the even and the odd buffers respectively buffer the outputs of the even and odd set of P/S converters so that the even and odd set of S/P converters receive the even and odd received serial data synchronous with the clock.

26. A bi-directional serial/parallel bus interface employed by a base station comprising:

a plurality of lines for transferring data blocks, the plurality of lines being less than a number of bits in each data block;

a first node sending first data blocks to a second node over the plurality of lines, the first node demultiplexing the data block into a plurality of first nibbles, the plurality of first nibbles being equal in number to the plurality of lines, each first nibble having a plurality of bits; and

the second node sending second data blocks to the first node over the plurality of lines, the second node demultiplexing the data block into a plurality of second nibbles, the plurality of second nibbles being equal in number to the plurality of lines, each second nibble having a plurality of bits.

27. The base station interface of claim 26 wherein the first node demultiplex the data block into a plurality of third nibbles, a number j of the third nibbles is less than the number N of lines and transferring the third nibbles over j lines.

28. The base station interface of claim 27 wherein the second node demultiplexes fourth data blocks into K bits, where K is less than or equal to N-j lines, and transferring the fourth data block over K lines.

29. The base station interface of claim 26 wherein the first node data blocks include gain control information.

30. The base station of claim 29 wherein the second node data blocks include an acknowledgment of receipt of the gain control information.

31. The base station interface of claim 29 wherein the second node data blocks include information of a status associated with the second node.

32. A gain control (GC) employed by a base station, comprising:

a GC controller for producing a data block having n bits representing a gain value;

i lines for transferring the data block from the GC controller to a GC, where $1<i<n$; and

the GC for receiving the data block and adjusting a gain of the GC using the gain value of the data block.

33. The base station GC of claim 32 further comprising:

a data block demultiplexing device for demultiplexing the data block into a plurality of nibbles, each nibble being transferred over a different line of the i lines; and

a data block reconstruction device for combining the nibbles into the data block.

34. The base station GC of claim 33 wherein appended to each nibble is a start bit.

35. The base station GC of claim 34 wherein the start bits indicate a function to be performed.

36. The base station GC of claim 35 wherein mathematical functions indicated by the start bits include a relative increase, a relative decrease and an absolute value function.

37. The base station GC of claim 34 wherein the GC includes a RX GC and a TX GC and the start bits indicate whether the data block is sent to the RX GC or TX GC.

GBH/LOU

PATENT COOPERATION TREATY

RECEIVED
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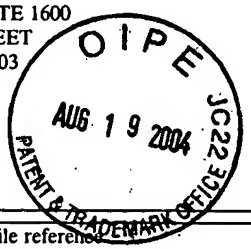
JUL 23 2004
VOLPE & KOENIG, P.C.

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
ANTHONY S. VOLPE
VOLPE AND KOEING, P.C.
UNITED PLAZA, SUITE 1600
30 SOUTH 17TH STREET
PHILAPHIA, PA 19103



PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	21 JUL 2004
Applicant's or agent's file reference: 1-2-0201.1WO	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US02/37150	19 November 2002 (19.11.2002)	21 November 2001 (21.11.2001)

Applicant

INTERDIGITAL TECHNOLOGY CORPORATION

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US	Authorized officer
Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Abdelmoniem Elamin Peggy Harwood Telephone No. (703)305-3804

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 1-2-0201.1WO	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/US02/37150	International filing date *(day/month/year)* 19 November 2002 (19.11.2002)	Priority date *(day/month/year)* 21 November 2001 (21.11.2001)
International Patent Classification (IPC) or national classification and IPC IPC(7): G06F 13/14 and US Cl.: 710/52, 74; 711/115		
Applicant INTERDIGITAL TECHNOLOGY CORPORATION		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 3 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of ___ sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
20 June 2003 (20.06.2003)	07 July 2004 (07.07.2004)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Abdelmoniem Elamin Telephone No. (703)305-3804

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/37150

I. Basis of the report

1. With regard to the **elements** of the international application:*

☒ the international application as originally filed.

☒ the description:
pages 1-9 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages 10-17, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the drawings:
pages 1-8, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages NONE

☐ the claims, Nos. NONE

☐ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US02/37150

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims 1-37	YES
	Claims NONE	NO
Inventive Step (IS)	Claims 1-37	YES
	Claims NONE	NO
Industrial Applicability (IA)	Claims 1-37	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS

Claim1-37 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest a parallel to serial converter for converting that nibble into serial data; a line for transferring that nibble serial data; and a serial to parallel converter for converting that nibble serial data to recover that nibble.

---------- NEW CITATIONS ----------

PTO/SB/21 (04-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/081,466
Filing Date	February 22, 2002
First Named Inventor	Gredone et al.
Art Unit	2182
Examiner Name	Abdelmoniem I. Elamin
Attorney Docket Number	I-2-0201.1US

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please Identify below):

COMMUNICATION RE FAVORABLE IPER BY IPEA/ US IN CORRESPONDING INTERNATIONAL APPLICATION; COPY OF APPROVED CLAIMS 1-57 AS PUBLISHED; AND COPY OF IPER

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Louis Weinstein Reg. No. 20,477 Volpe and Koenig, P.C.
Signature	
Date	August 17, 2004

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Louis Weinstein		
Signature		Date	8/17/04